

*AMENDMENTS TO THE CLAIMS*

This listing of claims replaces all prior versions, and listings, of claims in the application.

1. (Previously presented) A processing apparatus for processing data, based on control signals generated from a set of instructions being executed in parallel, comprising:

a plurality of issue slots, wherein each issue slot comprises a plurality of functional units, the plurality of issue slots being controlled by a set of control words, corresponding to the set of instructions,

wherein the processing apparatus further comprises a dedicated issue slot arranged for loading an immediate value in dependence upon a dedicated instruction comprising the immediate value, the processing apparatus further comprising a dedicated register file dedicated solely for said immediate value, the dedicated register file being accessible by the dedicated issue slot.

2. (Original) An apparatus according to claim 1, wherein the dedicated issue slot comprises a single functional unit arranged for only executing the dedicated instruction.

3. (Canceled)

4. (Original) An apparatus according to claim 1, wherein said processing apparatus is a VLIW processor and wherein said set of instructions is grouped in a VLIW instruction.

5. (Original) An apparatus according to claim 4, wherein the VLIW instruction is a compressed VLIW instruction, comprising dedicated bits for encoding NOP operations.

6. (Original) An apparatus according to claim 1, further comprising a register file associated with the plurality of issue slots.

7. (Original) An apparatus according to claim 6, further comprising a connection network for coupling the plurality of issue slots and the register file.

8. (Currently amended) A method for processing data, said method comprising:

storing input data in a register file;

processing data retrieved from the register file based on control signals generated from a set of instructions being executed in parallel, using a plurality of issue slots controlled by a set of control words being generated from the set of instructions; and wherein each issue slot comprises a plurality of functional units; and

loading an immediate value into a dedicated issue slot in dependence upon a dedicated instruction comprising the immediate value; and

passing the immediate value, received by the dedicated issue slot during the loading step, from the dedicated issue slot to a dedicated register file dedicated solely for said immediate value.

9-12. (Canceled)

13. (Previously Presented) The apparatus of claim 1, wherein the dedicated issue slot is controlled to load the immediate value by a control word consisting of the immediate value.

14. (Previously presented) The apparatus of claim 1, wherein the dedicated issue slot comprises a single functional unit arranged for only executing the dedicated instruction, and wherein the dedicated register file can be written to only by the single functional unit of the dedicated issue slot.

15. (Previously Presented) The apparatus of claim 14, wherein the single functional unit of the dedicated issue slot can only write to the dedicated register file.

16. (Previously Presented) The method of claim 8, wherein the dedicated issue slot is controlled to load the immediate value by a control word consisting of the immediate value.

17. (Previously Presented) The method of claim 8, further comprising executing the dedicated instruction with a single functional unit of the dedicated issue slot.

18. (Previously presented) The processing apparatus of claim 1, further comprising another register file separate from the dedicated register file, for storing input data and result data for the plurality of issue slots except for the dedicated issue slot.